

# Index

## 1

16L8, 127.  
PAL16L8, 127.

## 2

2732, 206, 426, 434–435, 453, 510–513, 529–532,  
674.

## 4

4-stage look-ahead circuit, 248.

## 6

6116, 427, 434–436, 453–456, 510–513, 529–531,  
658–660.  
68000 / 68HC000, 31, 198, 205, 218, 220–223,  
284–286, 457–542, 576–580, 585, 649–650.  
68008, 457–458.  
68010, 457–458.  
68012, 457–458.  
68020, 285, 354, 576–610.  
68030 / 68040 / 68060, 18, 285, 354, 576–577,  
610–611.  
6821, 514–517, 529–530, 652–657.  
68230, 516–520, 610, 651.

## 7

7447, 102.  
7448, 104.  
74HC00 / 74LS00, 58–59.  
74HC02 / 74LS02, 58–59.  
74HC04 / 74LS04, 54.  
74HC08 / 74LS08, 57.  
74HC138 / 74LS138, 113–114, 119.  
74HC151 / 74LS151, 119.  
74HC266 / 74LS266, 61–62.  
74HC283 / 74LS283, 119.  
74HC32 / 74LS32, 55–56.  
74HC373 / 74LS373, 143, 423.  
74HC86 / 74LS86, 61.  
74HCT244 / 74HCT245, 15.

## 8

80186 / 80188, 187, 368–369.  
80286, 369.  
80386, 369, 545–571.  
80486, 189, 198, 369, 545, 565–571.  
8086, 187, 200–201, 204–205, 211–212, 341–342,  
367–456, 671.  
8088, 368.

8255, 429–432, 434–436, 675.  
8284, 417–420, 672.  
8288, 673.

## A

A/D converter, 339–341, 344–345, 440–441,  
524–526, 579, 594, 634.  
ABEL, 128, 634.  
Accumulator, 188–189, 218, 634.  
Active high, 63.  
Active low, 63.  
Adder, 106–119, 244–251.  
BCD, 108–109  
Binary, 106, 119.  
Carry look ahead, 247–248.  
Carry save, 250, 347.  
Full, 106–107, 244, 246, 250, 638.  
Half, 105–108, 244.  
Ripple carry adder, 108.  
Adder / Subtractor, 119–120.  
Address, 3, 121, 123, 167, 187, 189, 204–205,  
216–218, 634.  
Addressing modes, 220, 373–376, 461–466,  
550–551, 583–587, 634.  
Address bus, 3, 187, 458.  
Algorithmic State Machines (ASM) Chart. *See* ASM  
charts.  
Alphanumeric codes, 32–34.  
Altera Quartus II, 129.  
AltiVec, 20, 619, 620.  
AltiVec vs. MMX, 620.  
ALU, 2, 37, 188–189, 254–257, 349–350, 634.  
Analog to Digital Converter. *See* A/D Converter.  
Analysis of a Combinational Logic Circuit,  
100–101.  
Analysis of a Synchronous Sequential Circuit,  
145–147.  
AND, 4, 55–58, 633.  
Arithmetic and logic unit. *See* ALU.  
Array multipliers, 252–253.  
Array processors, 349–351.  
ASCII, 33–34, 212, 378, 380–381, 383–384, 596,  
597, 601, 633.  
ASIC, 20–21, 634.  
ASM charts, 135, 168–176.  
Assemblers, 213–214, 223, 231, 633.  
Assembler Directives, 214–216, 396–399.  
Assembly Language, 210–223, 398, 400, 402–414,  
492–498, 559–560, 588–601, 634.  
Assembly Language Instruction Formats, 216–218.  
Assembly Language vs. C Language, 223  
Associative cache, 329.  
Asynchronous sequential circuit, 135, 176–178,  
184, 634.

**B**

Barrel shifter, 242–245, 354, 547, 570, 577, 634.  
 Basic Microprocessor Registers, 188–189.  
 BCD Adder, 108–109.  
 BCD Addition, 47–48, 483.  
 BCD Arithmetic, 47–48, 483.  
 BCD code, 33, 634.  
 BCD Subtraction, 48, 483.  
 BCD to seven-segment decoder, 101–105, 441.  
 BICMOS, 2, 18, 251, 546, 569.  
 Big-endian, 461.  
 Binary, 1, 24–33, 38, 46.  
 Binary Adders. *See* Adders, Binary.  
 Binary Arithmetic, 38–46.  
 Binary number, 1, 24, 28–32.  
 Bipolar junction transistor, 4, 6.  
 Bit, 2, 634.  
 BJT, 4, 6.  
 Block transfer DMA, 345–346.  
 Boolean algebra, 53, 64–65.  
 Boolean function, 64.  
 Boolean Identities, 65.  
 Breakpoint, 231, 437, 580, 602, 634.  
 Buffer, 6, 8, 15, 635.  
 Bus, 3, 186–187, 200, 260–263, 635.  
 Byte, 2.

**C**

C Language, 223–226, 400, 404, 411, 491, 495, 497.  
 C++, 1, 222–223, 226–227, 431–432, 520–521.  
 Cache, 326–335, 543–546, 565–569, 578, 583, 603, 605, 610.  
 Cache Memory, 326–335, 635.  
   Associative, 329, 331.  
   Direct Mapping, 328.  
   Efficiency, 330–331.  
   Hit Ratio, 327, 330–331.  
   Miss, 327, 331.  
   Motorola 68020 cache, 364, 543.  
   Organization, 326–335.  
   Set Associative, 329–330.  
   Valid bit, 330, 334.  
   Write-back, 330.  
   Write-through, 330.  
 CAD Tools, 20, 127.  
 Canonical forms, 71.  
 Carry flag, 38–49, 197–198, 379, 385, 460, 474, 549, 583.  
 Carry Look-ahead Adder. *See* Adder, Carry Look-ahead.  
 Carry Look-ahead Circuit, 248.  
 Carry Propagate adder, 245, 247.  
 Carry Save addition, 250.  
 CD-memories, 21, 300, 635.  
 Central processing unit. *See* CPU.

Characteristics table

D flip-flop, 142.  
 JK flip-flop, 142.  
 RS flip-flop, 142.  
 T flip-flop, 142.  
 Characteristic equation of D-FF, 144.  
 Characteristic equation of JK-FF, 144.  
 Characteristic equation of RS-FF, 144.  
 Characteristic equation of T-FF, 144.  
 Chip, 4, 635.  
 CISC, 240–241, 258–259, 545, 611, 635.  
 Clock, 4, 140, 164, 187, 268, 417–418, 503–504, 635.  
 CMOS, 13–17, 143, 635.  
 CMOS Inverter, 13–14.  
 Codes, 32–36.  
   Alphanumeric, 32–34.  
   ASCII, 33–34.  
   BCD, 33–34.  
   EBCDIC, 33–34.  
   Excess-3, 34–35.  
   Gray Code, 35–36.  
 Code Converter, 101–105.  
 Combinational logic circuit, 99–101, 635.  
   Analysis, 100–101.  
   Design, 101.  
 Combinational shifter, 242–244.  
 Combined paging/segmentation, 305.  
 Comparator, 110–112.  
 Compiler, 1, 223, 635.  
 Complement, 30, 32, 38–40, 70–71.  
 Complementary MOS. *See* CMOS.  
 Complement of a Boolean Function, 70–71.  
 Computer, 1, 186.  
 Computer Architectures, 348–349.  
 Computer Instructions, 237–239.  
 Consensus Theorem, 68–69.  
 Control bus, 3, 187, 198.  
 Control memory, 201–202, 258, 271–275, 284–286.  
 Control signals, 198–199.  
 Control Unit, 2, 198, 201–204, 237, 257–259, 262–264, 270–273, 275, 280, 285, 636.  
 Control Unit Design, 257–277.  
   Hardwired Control, 258, 263–270.  
   Microprogrammed Control, 258, 270–277.  
   Nanomemory, 284–286.  
 Counter, 156–161, 164–166, 735–740, 773–777.  
   Design, 156–161.  
   Johnson, 166.  
   Modulo-n, 164–166.  
   Ring, 165.  
   Self-correcting, 159.  
   Verilog, 735–740.  
   VHDL, 773–777.  
 CPLD, 126–128, 636.  
 CPU, 1–2, 185, 635.  
 CPU Design, 277–283.  
   ALU, 2, 37, 188–189, 254–257, 349–350, 457.  
   Control Unit, 2, 198, 200–204, 237, 257–259, 262–264, 270–273, 275, 280.  
   Register, 162–164, 242–244

Verilog, 129, 741–743.  
 VHDL, 777–778.  
 Cross Assembler, 213.  
 Cycle stealing DMA, 345–346, 347, 636.

## D

D Flip-Flop, 139, 142.  
 Characteristic table, 142.  
 Description, 139.  
 Excitation table, 142.  
 D/A, 2, 3, 19, 185, 636.  
 Daisy Chain Interrupt, 342, 344–345.  
 Data, 1, 189, 190–193, 636.  
 Data bus, 3, 187, 193, 423.  
 Data direction register, 336–337, 515.  
 Debouncer, 137.  
 Decoder, 112–114, 118–120, 636.  
 Define Byte (DB), 215.  
 Define Constant (DC), 215.  
 Define Word, 215–216.  
 Delay Routine, 399–400, 489–490.  
 Delimiters, 214.  
 DeMorgan's Theorem, 65–66, 70, 83.  
 Demultiplexers, 118, 636.  
 Design of a Combinational Circuit, 101.  
 Design of Counters, 156–161.  
 Design of Synchronous Sequential Circuits, 150–156.  
 Digital to Analog converter. *See* D/A.  
 Diode, 5, 6, 9, 11, 55–57, 121–122, 124, 636.  
 DIP, 16.  
 Direct cache mapping, 328.  
 Direct Memory Access. *See* DMA.  
 Distributive Law, 65–66.  
 Division of unsigned and signed numbers, 31, 46, 253–254.  
 DMA, 345–347, 440, 526, 634, 636.  
 Block Transfer, 345–346, 634.  
 Cycle Stealing, 345–346.  
 Interleaved, 345–346.  
 Don't Care Conditions, 83–85, 96, 160.  
 DRAM, 166, 206, 209, 637.  
 Dual of a Boolean Function, 65, 70–71.  
 Dual In-line Package. *See* DIP.  
 DVD, 21, 637.  
 Dynamic RAM. *See* DRAM.

## E

EPROM, *See* EEPROM.  
 EAROM, *See* EEPROM.  
 EBCDIC, 33–34, 637.  
 ECL, 9–10, 16.  
 EDO DRAM, 206.  
 EEPROM, 123, 127, 206, 637.  
 Embedded Application, 611.  
 Encoders, 115–116, 637.  
 EQU, 215.  
 Equivalence, 62, 637.

Error Correction and Detection, 49–50.  
 Essential prime implicants, 81–82.  
 Even function, 93–94.  
 Excess-3 Code, 34–35.  
 Excitation table, 142.  
 D flip-flop, 142.  
 JK flip-flop, 142.  
 RS flip-flop, 142.  
 T flip-flop, 142.  
 Exclusive-NOR, 61–62, 67, 93, 637.  
 Exclusive-OR, 60–61, 67, 88, 91, 93, 637.  
 Expanding op-code technique, 238–239.  
 External Interrupts, 341–345, 436–440, 521–526.

## F

Fan-out, 9.  
 Fetch timing diagram, 206–207.  
 Field Programmable Devices, 123–127.  
 Firmware, 258, 637.  
 Five-Variable K-map, 84–86.  
 Fixed-Point Numbers, 37.  
 Flag register, 197–198, 220, 277, 372–373, 460, 548–549, 741–743, 777–778.  
 Flash memory, 127, 207, 300, 638.  
 Flip-flops, 136, 138–144, 638.  
 D flip-flop, 139, 141–143.  
 JK flip-flop, 139–140, 143–144.  
 Master-Slave, 140–141.  
 Preset and Clear, 141–143.  
 RS flip-flop, 138–139, 142, 144.  
 Summary, 143–144.  
 T flip-flop, 140, 142–144.  
 Floating-Point Numbers, 37.  
 Floppy disk, 300.  
 Flowcharts, 228.  
 Foldback, 304.  
 Four-Variable K-map, 79.  
 FPGA, 127, 638.  
 Fragmentation, 306–307.  
 Full adder. *See* Adder, Full.  
 Full subtractor, 109–110  
 Fully associative cache mapping, 329.

## G

Gates, 4, 54, 638.  
 Gates with multiple inputs, 66–67  
 General-purpose Resister-based Micorprocessor, 189.  
 General-purpose Register, 162–164, 182, 189, 193.  
 Glitch, 70.  
 Gray Code, 35–36.

## H

Half-Adder. *See* Adder, Half.  
 Half subtractor, 109.  
 Hardware, 1, 638.  
 Hardware breakpoint, 231.

Hardware Description Language, 127–129.  
 Behavioral, 128, 719–720.  
 Dataflow, 128, 719.  
 Structural, 128, 717–719.  
 Hardwired control, 263–270, 638.  
 Hard disk, 300.  
 Hazard, 70.  
 HCMOS, 2, 18, 251, 457, 504, 547, 563, 638.  
 HCT chips, 14.  
 HDL. *See* Hardware Description Language.  
 Hexadecimal Numbers, 25, 27–28, 638.  
 High-level language, 222–227, 638.  
 High-speed CMOS. *See* HCMOS.  
 HMOS, 18, 286, 457, 638.

**I**

I/O, 185–186, 335–347, 428–432, 436–446,  
 514–526.  
 DMA, 345–347, 440, 526.  
 Interrupt I/O, 336, 340–345, 436–446, 521–526.  
 Programmed I/O, 335–346, 428–432, 514–521.  
 I/O summary, 347.  
 IC, 4.  
 IEEE Symbols for Logic Gates, 62.  
 Index Register, 194, 375, 462, 464–465.  
 Input/Output. *See* I/O.  
 Instruction, 1, 218–219, 238–239, 376–395,  
 467–487, 551–558, 587–601, 639.  
 Instruction Encoding, 237–239.  
 Block code, 237.  
 Expanding opcode, 237–239.  
 Instruction Fetch Timing Diagram, 206–207.  
 Instruction format, 216–218.  
 Instruction Register, 188, 190–193, 639.  
 Instruction Set. *See* Instruction.  
 Integrated Circuit. *See* IC.  
 Intel 32- and 64-bit microprocessors, 545–546.  
 Intel 80186, 368.  
 Intel 80188, 368.  
 Intel 80286, 369.  
 Intel 80386, 546–565.  
 Addressing Modes, 550–551.  
 Data types, 548–549.  
 Dynamic Bus sizing, 562.  
 Functional units, 547.  
 I/O, 564–565, 639.  
 Instruction Set, 551–558.  
 Memory Organization, 548.  
 Pins and Signals, 560–561.  
 Registers, 549–550.  
 System Design, 562–564.  
 Intel 80386 vs. 80486, 566.  
 Intel 80486, 565–568.  
 Intel 8086-based Microcomputer schematic, 433.  
 Intel 8086, 200, 367–451, 701–711.  
 Addressing modes, 373–376.  
 Assembler directives, 396–399.  
 C Programming Example, 400–401, 404,  
 411–412, 431–432.  
 Clock generation, 418.  
 Delay routine, 399–400.  
 Demultiplexing address/data bus using 74LS373,  
 423.  
 Display Interface, 446–450.  
 DMA, 440.  
 Functional units, 200–201.  
 I/O ports, 428–432.  
 I/O map, 435–436.  
 Instruction set, 376–395, 701–711.  
 Interfacing with memories, 425–428.  
 Interrupts, 436–440.  
 Keyboard / Display Interface, 446–451.  
 Memory map, 434–435.  
 Memory & I/O interface, 434–436.  
 Microcomputer schematic, 433.  
 Pins and Signals, 414–417.  
 Programming examples, 400–414.  
 Ready, 420.  
 Registers, 370–373.  
 Reset, 419–420.  
 Stack, 399.  
 System Design, 434–436.  
 Timing Diagram, 421–422.  
 Intel 8284, 418–420, 672.  
 Intel 8255, 429–430, 434–436, 675.  
 Intel Merced/IA/64, 18, 20, 575.  
 Intel Pentium, 18, 545, 568–572.  
 Intel Pentium II / Celeron / Xeon, 573–574.  
 Intel Pentium III / Pentium 4, 574–575.  
 Intel Pentium Pro, 572–573.  
 Interleaved DMA, 345–346, 639.  
 Internal interrupts, 341–342, 639.  
 Interrupt Address Vector, 342.  
 Interrupt I/O, 340–345, 436–446, 521–526, 639.  
 Interrupt Priorities, 342–345.  
 Interrupt service routine, 340–341, 343.  
 Interrupt Types, 341.  
 Inverter, 4, 7, 53–54.

**J**

Java, 227.  
 JK Flip-Flop, 139–140, 142.  
 Characteristic table, 142.  
 Description, 139–140.  
 Excitation table, 142.  
 Johnson Counter, 166.

**K**

K-map. *See* Karnaugh Maps.  
 Karnaugh Maps, 75–86, 639.

**L**

L1 Cache, 335.  
 L2 Cache, 335, 573, 574.  
 Latches, 136.  
 LED, 7–9, 640.

- Light Emitting Diodes. *See* LED.  
 Literal, 65.  
 Little-endian, 370.  
 Locality of reference, 326.  
 Logical shift operation, 162.  
 LS-TTL, 9–10, 14–16, 504.  
 LSI, 15–16, 20–21, 640.
- M**
- Machine language, 210–212, 640.  
 Macroassembler, 213.  
 Macroprogram, 202.  
 Main memory, 187, 204–205, 299–304, 369–370, 644.  
 Main Memory Array Design, 300–304.  
 Maskable interrupts, 341–342, 347, 438–440, 521–526.  
 Masking operation, 219, 384–385, 477–478.  
 Master-Slave Flip-Flop, 140–141.  
 Maxterms, 71, 72, 73, 74, 75, 83.  
 MC6116, 427, 433–435, 510, 512–513, 658–660.  
 MC68000, 31, 198, 205, 218, 220–223, 284–286, 457–542, 576–580, 585, 649–650.  
 MC68008, 458.  
 MC68010, 458.  
 MC68012, 458.  
 MC6821, 514–517, 652–657.  
 MC68230, 516–520, 651.  
 Mealy circuit, 148.  
 Memory, 1, 3, 121–123, 166–168, 185, 204–209, 434–435, 511–514, 548, 607–610, 640.  
 Memory Address Register, 189, 641.  
 Memory fragmentation, 306, 307.  
 Memory management, 304–307.  
 Memory Management Unit, 305–306, 641.  
 Memory mapped I/O, 337–338, 347, 428–429, 456, 514–521, 641.  
 Memory Organization, 209, 299.  
 Memory Types, 3, 121, 123, 127, 166–168, 205–209, 326–335.  
   Cache, 326–335.  
   DRAM, 166, 206, 209.  
   E<sup>2</sup>PROM, 123, 127, 206, 637.  
   EAROM, 123, 127, 206, 637.  
   EEPROM, 123, 127, 206, 637.  
   Nonvolatile, 3, 121.  
   PROM, 123.  
   RAM, 3, 166–168, 205–209.  
   ROM, 121, 123.  
   SRAM, 166, 205.  
   Volatile, 3, 166, 205.  
 Merced, 18, 20, 575.  
 Meta-assembler, 214.  
 Metal-Oxide Semiconductor, 4, 13.  
 Microcomputer, 2, 185–189, 433, 528, 641.  
 Microcomputer Bus. *See* Bus.  
 Microcomputer Development Systems, 228–231.  
 Microcomputer programming languages, 210.  
 Microcontrollers, 2, 185–186, 641.  
 Microinstruction, 201, 270–277, 641.  
 Microprocessor, 1, 2, 185, 188–201, 641.  
 Microprocessor registers, 188–189, 193–198.  
 Microprocessor system development flowchart, 232–233.  
 Microprogram, 201–204, 270–283, 641.  
 Microprogrammed Control Unit Design, 270–283.  
 Microprogrammed CPU Design, 277–283.  
 Microprogramming, 201–204, 270–283.  
 Minterms, 71–74.  
 MIPS, 545.  
 MMU. *See* Memory Management Unit.  
 MMX, 573–574, 619–620.  
 Modulo-4 Counter, 166.  
 Modulo-n Counters, 164.  
 Monitors, 227–228.  
 Moore circuit, 148.  
 MOS, 1–2, 13–15.  
 MOS outputs, 15.  
 MOS switch input, 15.  
 Motorola 32- and 64-bit microprocessors, 576–620.  
 Motorola 68000-based microcomputer schematic, 528.  
 Motorola's stat-of-the art microprocessors, 619–620.  
 Motorola 6116. *See* MC6116.  
 Motorola 68000-based Microcomputer, 529–532.  
 Motorola MC68000/68HC00, 457–542, 696–699.  
   Addressing Modes, 461–466.  
   C Programming Example, 491–492, 495, 497, 520–521.  
   Clock Generation, 504–505.  
   DELAY Routine, 489–490.  
   DMA, 526.  
   DTACK delay circuit, 529.  
   DTACK timing diagram, 529.  
   Exceptions, 526–529.  
   Programming examples, 490–498.  
   I/O map, 517, 519.  
   Instruction Execution Times, 661–669.  
   Instruction Set, 467–487, 696–699.  
   Interfacing with Memories, 511–514.  
   Interrupts, 521–526.  
   Memory Addressing, 461.  
   Memory map, 513.  
   Microcomputer, 528–532.  
   Microcomputer schematic, 528.  
   Multiprocessing, 531–532.  
   Pins and Signals, 499–503.  
   Programmed I/O, 514–521.  
   Registers, 460.  
   Reset, 505–509.  
   68000-6821 Interface, 515–517.  
   6800-68230 Interface, 517–519.  
   Stack, 487–489.  
   System Design, 528–532.  
   Timing Diagrams, 508–511.  
 Motorola MC68008, 458.  
 Motorola MC68010, 458.  
 Motorola MC68012, 458.  
 Motorola MC6821, 514–517.

Motorola MC68020, 576–610.  
 Addressing Modes, 583–587.  
 Comparison with 68HC000, 576.  
 Dynamic Bus Sizing, 604–605.  
 I/O, 610.  
 Instruction Set, 587–601, 695–699.  
 Interfacing with Memories, 607–610.  
 Pins and Signals, 601–604.  
 Registers, 581–583.  
 System Design, 607–610.  
 Motorola MC68030, 610.  
 Motorola MC68040 / MC68060, 610–611.  
 Motorola MC68230, 516–520.  
 Motorola PowerPC. *See* PowerPC.  
 MSI, 15, 16.  
 Multiple-Output Combinational Circuits, 102, 105.  
 Multiplexer, 116–118, 641.  
 Multiplication of two unsigned and signed binary numbers, 46, 250–254.  
 MUX. *See* Multiplexer.

## N

NAND, 15, 16, 58–59, 63, 67, 88–91, 642.  
 NAND gate implementation, 88–91.  
 Nanomemory, 284–286, 642.  
 Nanoprogram. *See* Nanomemory.  
 Negative logic, 63.  
 Nibble, 2, 642.  
 Nine's complement, 39.  
 NMOS, 13.  
 Noise margin, 10.  
 Nonmaskable interrupts, 341, 437, 521, 642.  
 Nonvolatile memory, 3, 121.  
 NOR, 58, 59, 91–93, 642.  
 NOR gate implementation, 91–93, 642.  
 NOT, 4, 6, 7, 12–13, 53–54, 642.  
 Number Systems, 23–52.  
 Binary, 24, 26–28.  
 Hexadecimal, 25, 27–28.  
 Octal, 24, 25.  
 Signed, 29–32.  
 Unsigned, 28–31.

## O

Object codes, 211, 642.  
 Octal Number, 24, 25, 642.  
 Odd Function, 93.  
 One-Pass Assembler, 213, 642.  
 Ones complement, 29, 39–40, 54, 642.  
 Ones complement arithmetic, 39–40.  
 Op-code encoding, 237–239.  
 Open-collector outputs, 10–11.  
 Operating systems, 226, 300, 305, 336, 458, 544, 643.  
 Optical memories, 21, 300.  
 OR, 4, 54–56, 643.  
 ORG, 215.  
 ORIGIN. *See* ORG.

Overflow, 43–46, 250, 379, 474.

## P

Packed BCD, 33–34, 381, 383, 482–483, 596–597.  
 Paged-segmentation method, 307.  
 Paging, 305, 307–309, 311–315, 318, 643.  
 PAL, 124, 126–128, 644.  
 PAL16L8, 127.  
 Parallel processing, 347–359.  
 Parity, 49–50, 93–94, 643.  
 PEEL, 127.  
 Pentium, 18, 545, 568–572, 644.  
 Pentium II, Pentium III, Pentium 4, 573–575.  
 Pentium Pro, 572–573.  
 PGA, 16.  
 Pin Grid Array. *See* PGA.  
 Pipelining, 258, 351–359, 643.  
 Arithmetic pipeline, 353–354.  
 Instruction pipeline, 354–359.  
 PLA, 124–126, 132, 644.  
 PLDs, 123–124, 127, 644.  
 PLD Programming Languages, 127–129.  
 PMOS, 13.  
 Polled interrupt, 342–344, 643.  
 POP, 196–197, 222, 399, 487–489, 643.  
 Port, 336–340, 639, 643.  
 Positive logic, 63.  
 PowerPC, 18, 37, 189, 258, 544–545, 576, 611–620.  
 Preset and Clear Inputs of Flip-Flops, 141–143.  
 Primary memory, *See* Main Memory.  
 Prime Implicants, 81–83.  
 Priority Encoder, 114–116.  
 Processor memory, 299, 644.  
 Product-of-sums, 73–74.  
 Program, 1, 189–193, 644.  
 Programmable array logic. *See* PAL.  
 Programmable logic array. *See* PLA.  
 Programmable Logic Devices. *See* PLD.  
 Programmed I/O, 335–346, 428–432, 514–521, 644.  
 Program Counter, 188–191.  
 PROM, 123, 644.  
 Propagation delay, 9–10.  
 PUSH, 196–197, 222, 399, 487–489, 644.

## Q

Quine-McCluskey Method, 86–87.

## R

RAM, 3, 166–168, 205–209, 644.  
 Random Access Memory. *See* RAM.  
 Race Condition, 70.  
 Read-Only Memory. *See* ROM.  
 READ/WRITE, 198–199.  
 READY, 199.  
 READ and WRITE Operations, 207–209.

READ Timing Diagram, 207.  
 Register, 162–164, 242–244, 645.  
 Register transfer, 259–260.  
 Relocatable, 221.  
 RESET, 188–189, 419–420, 505–509.  
 Ring Counter, 165.  
 Ripple Carry Adder, 108.  
 Ripple Counter, 754.  
 RISC, 18, 239–242, 258, 545, 611–612, 644.  
 ROM, 121, 123, 644.  
 ROM-based multiplier, 251.  
 RS Flip-Flop, 138–139, 142, 144..  
   Characteristic table, 142.  
   Description, 138.  
   Excitation table, 142.

## S

Scalar Processor, 570, 645.  
 Schmitt Trigger, 419–420, 507, 645.  
 SDRAM, 206, 645.  
 Secondary memory, 299–300, 304–326, 645.  
 Segmentation, 305–308, 311–315.  
 Segmented memory, 204–205, 313–314, 316, 369.  
 Segments, 204–205, 305–306, 311–314.  
 Self-correcting counter, 159.  
 Sequential logic circuit, 172, 645.  
   Analysis, 145–147.  
   Design, 150–156.  
   Minimization, 148–150.  
 Set-associative cache mapping, 329–330.  
 Seven Segment Displays, 8.  
   Common anode, 8.  
   Common cathode, 8.  
 Shift Operations, 162–164, 384–386, 479–482.  
 Signed addition, 250–251.  
 Signed binary numbers, 29–32.  
 Signed division, 254.  
 Signed multiplication, 253–254.  
 Signed subtraction, 251.  
 Sign extension, 221, 383, 476.  
 Sign-magnitude arithmetic, 38.  
 Sign-magnitude Numbers, 29.  
 SIMD, 348–349.  
 Single-chip microcomputer, 2, 185, 645.  
 Single-Chip Microprocessor, 185, 188, 645.  
 Single-step, 231, 373, 437, 460, 646.  
 Sixty-Four Bit Microprocessors, 545, 575, 576, 619.  
 Software, 1, 228–233, 646.  
 Software breakpoint, 231.  
 Spooling, 336.  
 SRAM, 166, 205.  
 SRAM cell, 167.  
 SR Latch, 136–138.  
 SSI, 15–16.  
 Stack, 195–197, 372, 399, 487–489, 646.  
 Stack Pointer, 195, 197, 399, 460, 646.  
 Standard I/O, 337–338, 428, 565, 646.  
 State diagram, 147–154, 158–159.

State machines, 135, 170.  
 State machine design using ASM chart, 170–176.  
 State table, 146, 147.  
 Static RAM. *See* SRAM.  
 Status Register, 194–195, 197–198, 372–373, 460.  
 Subroutine, 221–222, 388–391, 485.  
 Subtractor,  
   Full-subtractor, 109–110.  
   Half-subtractor, 109.  
   One's complement, 39–40.  
 Sum-of-Products, 72, 74, 88.  
 Superscalar Processor, 570, 612, 646.  
 Synchronous sequential circuit, 145–176, 647.

## T

T Flip-Flop, 140, 142, 143, 144.  
   Characteristic table, 142.  
   Description, 140.  
   Excitation table, 142.  
 Ten's complement, 39.  
 Thirty-two Bit Microprocessors, 543, 576–611.  
 Three-Variable K-map, 76–77.  
 Totem-pole outputs, 10, 11.  
 Transistor, 1, 6–7, 647.  
   Active mode, 6.  
   Cut-off mode, 6.  
   Saturation mode, 6.  
 Tristate, 10, 11.  
 TTL, 9–11, 16, 17.  
 TTL Outputs, 10–11.  
   Open-collector output, 10, 11.  
   Totem-pole output, 10, 11.  
   Tristate, 10, 11.  
 Two-Pass Assembler, 213.  
 Two-Variable K-map, 76.  
 Twos complement, 39–46, 647.

## U

Unicode, 36–37.  
 Unified cache, 328.  
 Unpacked BCD, 32, 34, 381, 383, 405.  
 Unsigned addition, 38.  
 Unsigned binary numbers, 28–29.  
 Unsigned division, 46.  
 Unsigned multiplication, 46.  
 USB Flash Memory, 300.

## V

Vector machine, 349–351.  
 Verilog, 127–129, 647, 713–755.  
   ALU, 743–745.  
   always, 714, 715.  
   assign, 719, 729.  
   begin, 714.  
   Behavioral, 128, 129, 634, 719–721.  
   Blocking assignment, 730.  
   case, 720.

- Clock, 729.
  - Combinational circuit design, 721–728.
  - Concatenate operator, 719, 723.
  - Conditional operator, 714, 719.
  - Counter, 735–740.
  - CPU, 745–753.
  - Dataflow, 128, 636, 719.
  - $\$display$ , 716.
  - $\$monitor$ , 716.
  - $\$time$ , 715.
  - end, 714.
  - endmodule, 713.
  - Hierarchical, 714, 725.
  - if-else, 720.
  - initial, 714, 715, 729.
  - Memory, 743.
  - Miswiring, 715
  - module, 713.
  - Named association, 718.
  - Net, 713, 714.
  - Non-blocking assignment, 729.
  - Numbers, 714.
  - Operators, 719.
  - parameter, 714.
  - Positional association, 718.
  - Procedural statement, 729.
  - Reduction operator, 714.
  - reg, 714.
  - Register, 729.
  - Sequential circuit design, 728.
  - Status Register, 741–743.
  - Structural, 128, 717–719.
  - Test bench, 715.
  - User-Defined Primitive (UDP), 716.
  - wire, 713.
  - VHDL, 127–129, 648, 757–806.
    - ALU, 781–785.
    - architecture, 758.
    - Behavioral, 128, 129, 634, 761–763.
    - bit\_vector, 758.
    - buffer, 758.
    - case, 758.
    - Clock, 769.
    - Combinational circuit design, 766–769.
    - component, 761.
    - Concatenate operator, 764.
    - constant, 760.
    - Counter, 773–777.
    - CPU, 785–805.
    - Dataflow, 636, 763–765.
    - entity, 758.
    - generate, 778–781.
    - generic, 778–781.
    - generic map, 778–781.
    - Hierarchical, 759.
    - IEEE 1164, 758, 760.
    - if-else, 762, 763.
    - in, 758.
    - inout, 758.
    - Mixed, 765.
    - Named association, 761.
    - Operators, 757, 758.
    - out, 758.
    - port, 757.
    - Positional association, 761.
    - process, 762, 769.
    - signal, 760, 762.
    - Status Register, 777–778.
    - Structural, 759–761.
    - Synchronous sequential circuit design, 769–805.
    - variable, 760, 762.
    - wait until, 777.
    - when-else, 763–764.
    - with-select, 763, 764–765.
  - Virtual memory, 304–326, 648.
  - VLSI, 15–16.
  - Volatile memory, 3, 166, 205.
- ## W
- Wired-AND logic, 10, 11.
  - Word, 2, 3, 648.
  - Write-back method, 330.
  - Write-through method, 330.
  - WRITE Timing Diagram, 208, 209.
- ## X
- XNOR. *See* Exclusive-NOR.
  - XOR. *See* Exclusive-OR.
  - XOR/XNOR Implementation, 91–94.
- ## Z
- Zero flag, 195, 197–198, 373, 460.
  - Zip disk, 300.