

APPENDIX

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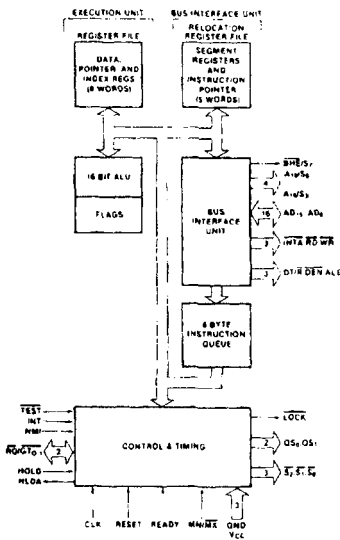
INTEL 8086 AND SUPPORT CHIPS



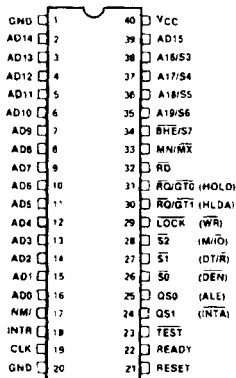
8086/8086-2/8086-4
16-BIT HMOS MICROPROCESSOR

- Direct Addressing Capability to 1 MByte of Memory
- Assembly Language Compatible with 8080/8085
- 14 Word, By 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Operations
- 8-and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide
- 5 MHz Clock Rate (8 MHz for 8086-2) (4 MHz for 8086-4)
- MULTIBUS™ System Compatible Interface

The Intel® 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance.



8086 CPU Functional Block Diagram



40 LEAD

8086 Pin Diagram

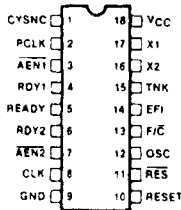


I8284
CLOCK GENERATOR AND DRIVER
FOR 8086, 8088, 8089 PROCESSORS

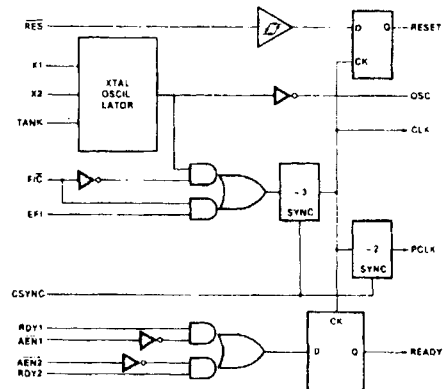
- Generates the System Clock for the 8086, 8088 and 8089
- Uses a Crystal or a TTL Signal for Frequency Source
- Single +5V Power Supply
- 18-Pin Package
- Generates System Reset Output from Schmitt Trigger Input
- Provides Local Ready and MULTIBUS™ Ready Synchronization
- Capable of Clock Synchronization with other 8284's
- Industrial Temperature Range
-40° to +85°C

The I8284 is a bipolar clock generator/driver designed to provide clock signals for the 8086, 8088 & 8089 and peripherals. It also contains READY logic for operation with two MULTIBUS™ systems and provides the processors required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided.

I8284 PIN CONFIGURATION



18284 BLOCK DIAGRAM



18284 PIN NAMES

X1	CONNECTIONS FOR CRYSTAL
X2 ¹	
TANK	USED WITH OVERTONE CRYSTAL
F/C	CLOCK SOURCE SELECT
EFI	EXTERNAL CLOCK INPUT
CSYNC	CLOCK SYNCHRONIZATION INPUT
RDY1 ²	
RDY2 ²	READY SIGNAL FROM TWO MULTIBUS™ SYSTEMS
EN1 ²	
EN2 ²	ADDRESS ENABLED QUALIFIERS FOR RDY1, 2
RES	RESET INPUT
RESET	SYNCHRONIZED RESET OUTPUT
OSC	OSCILLATOR OUTPUT
CLK	MOS CLOCK FOR THE PROCESSOR
PCLK	TTL CLOCK FOR PERIPHERALS
READY	SYNCHRONIZED READY OUTPUT
VCC	+5 VOLTS
GND	0 VOLTS

intel®

8288

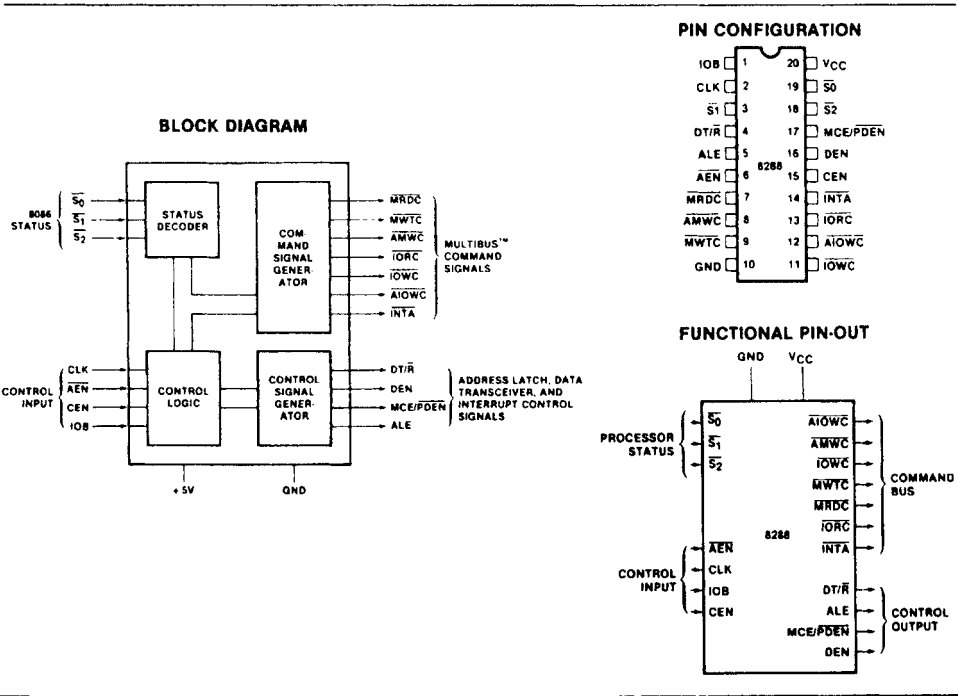
BUS CONTROLLER

FOR 8086, 8088, 8089 PROCESSORS

- Bipolar Drive Capability
 - Provides Advanced Commands
 - Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers
 - Configurable for Use with an I/O Bus
 - Facilitates Interface to One or Two Multi-Master Busses

The Intel® 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large 8086 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.



2732 32K (4K x 8) UV ERASABLE PROM

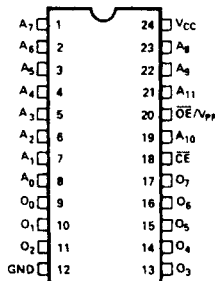
- **Fast Access Time:**
 - 450 ns Max. 2732
 - 550 ns Max. 2732-6
- **Single +5V \pm 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
 - 150mA Max. Active Current
 - 30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
 - Single Location Programming
 - Programs with One 50ms Pulse
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable (\overline{OE}), from the Chip Enable control (\overline{CE}). The \overline{OE} control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the \overline{OE} and \overline{CE} controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the \overline{CE} input.

PIN CONFIGURATION



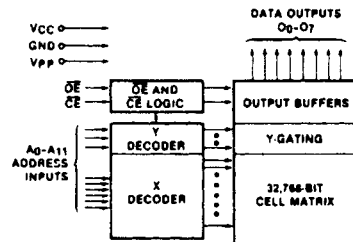
PIN NAMES

A ₀ -A ₁₁	ADDRESSES
\overline{CE}	CHIP ENABLE
\overline{OE}	OUTPUT ENABLE
O ₀ -O ₇	OUTPUTS

MODE SELECTION

MODE \ PINS	\overline{CE} (18)	\overline{OE}/V_{pp} (20)	V _{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V _{IL}	V _{IL}	+5	D _{OUT}
Standby	V _{IH}	Don't Care	+5	High Z
Program	V _{IL}	V _{pp}	+5	D _{IN}
Program Verify	V _{IL}	V _{IL}	+5	D _{OUT}
Program Inhibit	V _{IH}	V _{pp}	+5	High Z

BLOCK DIAGRAM



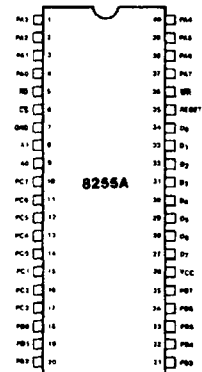


8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Micro-processor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

PIN CONFIGURATION



PIN NAMES

D ₇ -D ₀	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A ₀ , A ₁	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V _{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM

