APPENDIX

A

ANSWERS TO SELECTED PROBLEMS

Chapter 2

2.1(b) $1101.101_2 = 13.625_{10}$
2.2(b) $343_{10} = 101010111_2$
2.3(a) $1843_{10} = 3463_8$
2.4(b) $3072_{10} = C00_{16}$
2.6(c) $-48_{10} = 1101\ 0000_2$
2.11(c) $61440_{10} = 1001\ 0100\ 0111\ 0111\ 0011_2$
2.16(b) $0011\ 1110_2$
2.19(b) 0; no overflow
2.19(d) overflow
2.22(a) $0001\ 0000\ 0010_2$ = 102 in BCD

Chapter 3

3.1 $36_{16} \oplus 2A_{16} = 1C_{16}$
3.3 1's Complement of $A7_{16}$
3.4(d)
$$\overline{(A + \overline{A}B)} = \overline{A}\,\overline{(\overline{A}B)}$$
$$= \overline{A}\,(A + \overline{B})$$
$$= \overline{A}\,\overline{B}$$
3.4(f)
$$\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{C} = \overline{C}(\overline{B} + \overline{A}) + ABC$$
$$= \overline{C(\overline{AB})} + (AB)C$$
$$= \overline{C \oplus (AB)}$$
3.5(c) BC
3.7(a) $\overline{F} = \prod M(0, 1, 5, 7, 10, 14, 15)$
3.9(c) $F = \overline{Z}$
3.10(b) $F = BC + \overline{A}B$
3.11(d) $F = W \oplus Y$
3.11(e) F = Z
3.14(a) $f = A + \overline{B}C + B\overline{C}$
3.14(c) $f = \overline{B}$
3.15 $F = \overline{\overline{A}\,\overline{C} + \overline{C}\,\overline{D}}$
3.17(b) $F = \overline{\overline{(A + C)} + (B + \overline{C})}$

Chapter 4

4.1 F = 0
4.3(c) $F = A\overline{C} + BC$
4.7 $f = \overline{A \oplus C}$
4.10 $f_3 = \overline{A}\,\overline{B}\,\overline{C}$, $f_1 = \overline{C}$
$f_2 = B \oplus C$ $f_0 = \overline{D}$
4.13 Add the 4-bit unsigned number to itself using full-adders.

4.16 $Z = 1$
$Y = 0$
$X = m5$
$W = m9$

4.20 For 4-Bit signed number, A
$A + 1111_2 = A - 1$, decrement by 1.
$A + 0001_2 = A + 1$, increment by 1.
Manipulate C_{in} to accomplish the above.

Chapter 5

5.5 A = 1, B = 0

5.7 A = 1, B = 1

5.9

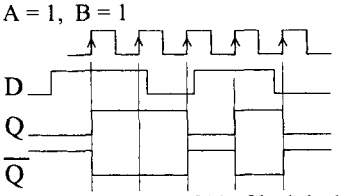


Figure for solution 5.9

5.13 Tie JK inputs to HIGH ; Clock is the T input.

5.15 $B_+ = A$, *output* $y = \overline{B}$

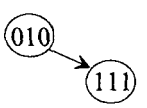
5.17(b) $Jx = z$, $kx = y$
$Jy = 1$, $ky = x + z$
$Jz = \overline{xy}$, $kz = x$

5.19 $D_A = (A \oplus x) + \overline{B}x$
$D_B = x(\overline{A \oplus B}) + A\overline{B}x$
Where x is the input

5.20(c) $Tx = \overline{y}$
$Ty = 1$

5.23 $T3 = Q_3Q_0 + Q_2Q_1Q_0$

5.24(a) $J_A = B$, $K_A = BC$, $J_B = C$, $K_B = C$, $J_C = 1$, $K_C = A + B$
self correcting



Chapter 6

6.4(a) sign = 0, carry = 0, zero = 0, overflow = 0.
(d) sign = 1, carry = 0, zero = 0, overflow = 1.

6.6(a) 20BE
(b) (20BE) = 05, (20BF) = 02

6.13(a) 16,384
(b) 128 chips
(c) 4 bits

6.18 Use the following identities: $a \oplus a = 0$ and $a \oplus 0 = a$ and $(a \oplus b) \oplus a = b$

Chapter 7

7.2 Yes, it is possible

7.5 Yes, it is possible

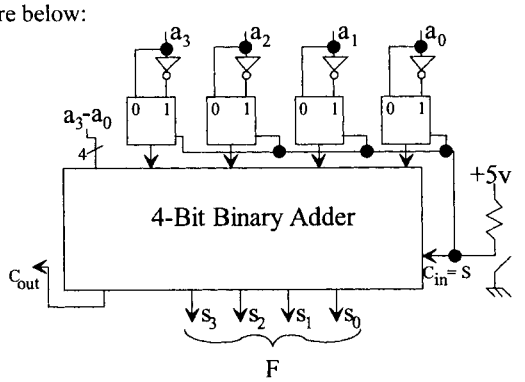
7.6 Use four mux's. Manipulate inputs of the mux's to obtain the desired outputs. Use the tristate buffers at the outputs of the mux's.

7.9 $y = |x|$
If $x_7 = 0$, then $y_7....y_2y_1y_0 = x_7....x_2x_1x_0$
else $y_7....y_2y_1y_0 = \overline{x}_7....\overline{x}_2\overline{x}_1\overline{x}_0 + 1$

use XOR gates for finding 1's complement of x .

7.11(a) $s_{15} \underset{3\Delta}{\leftarrow} c_{15} \underset{2\Delta}{\leftarrow} c_{12} \underset{2\Delta}{\leftarrow} g_i p_i \underset{2\Delta}{\leftarrow} G_i P_i \underset{\Delta}{\leftarrow} \begin{matrix} x_i \\ y_i \\ c_0 \end{matrix}$; worst case add-time: 10Δ

7.14 Refer to figure below:



7.17 Product = 0000 0000 0000 0100_2

7.22(a) $P_0 = \overline{Z}T_3$, $P_1 = T_5$

$L = P_0 + P_1$, $d_2 = P_1$, $d_1 = P_0$, $d_0 = P_1$

$C_0 = C_1 = T_0$, $C_2 = T_1$, $C_3 = C_4 = C_6 = T_2$, $C_5 = T_4$

7.25(a) Savings = 34,304 bits

7.34(a)

	C_4	C_3	C_2	C_1	C_0	
Solution 1	1	0	1	0	0	; A ← A minus A
Solution 2	1	1	1	0	0	; A ← A ex-or A

7.42 *Step 1:* Make F=0 (set $c_{10}c_{11}c_{12}$ to 000) and set the zero flag to 1.
Step 2: Execute JZ instruction.

Chapter 8

8.5 Memory Chip #1 EC00H - EDFFH
Memory Chip #2 F200H - F3FFH

8.6(a) ROM Map: 0000H - 07FFH
RAM Map: 2000H - 27FFH

8.13 20

8.14 Maximum Directly Addressable Memory = 16 Megabytes;
14 unused address pins Available.

8.16 (b)

Virtual address	Physical address
24	24
3784	1224
10250	page fault
30780	page fault

8.18 (a) 4/15

8.21 6 x 64 decoder

8.24 Cache Tag Field = 1-bit
Cache Index Field = 12-bits
Cache Data Field = 32-bits

8.26 Cache word size = 36 bits.

8.27 (a) 512 (e) $h = 0.85$

8.28 (b) Cache size is 4K words.
4 blocks per set.

8.37 (a) Pipeline clock rate = 5 MHz
(c) Efficiency = 99.8%

8.39 (a) Avg. number of instructions executed per instruction cycle ≅ 4.98

8.41 (a)

```
        LDA X
        JMP     2040
        DCR     Y
        SUB Z
          :
2040    STA W
```

The above program assumes that the system supports delayed branch.

Chapter 9

9.4 20642H

9.6(a) Implied

9.8 (AL) = 5

9.13

```
        XCHG    BL,BH
        MOV     AX,BX
        ADD     AX,CX
        HLT
```

9.19

```
        MOV     AL,CH
        CBW
        IDIV    CL
        MOV     CL,AH
        MOV     CH,AL
        HLT
```

9.26

```
CONV            SEGMENT
                ASSUME    CS:CONV
BCD2BIN         PROC    FAR
                MOV     BX,4000H
                MOV     CL,10
                MOV     DX,0
                MOV     AL,[BX]
                MUL     CL
                ADD     DX,AX
                INC     BX
                ADD     DL,[BX]
                RET
BC2BIN          ENDP
CONV            ENDS
                END
```

9.27

```
                MOV     CL,4
                MOV     AL,90H
                OUT     CNTRL,AL
                MOV     BL,0
BACK:           IN      AL,PORTA
```

```
                    RCR     AL,1
                    JC      START
                    INC     BL
        START: DEC  CL
                    JNZ     BACK
                    RCR     BL,1
                    JNC     LEDON
                    MOV     AL,0
                    OUT     PORTB,AL
                    HLT
        LEDON: MOV  AL,10H
                    OUT     PORTB,AL
                    HLT
```

9.28 Port A = 01H, Port B = 03H, Port C = 05H, CNTRL = 07H
2732 ODD = 00001H,00003H,...,01FFFH
2732 EVEN = 00000H,00002H,...,01FFEH

9.34 For 15 sec. delay: a count of 0931H provides a delay of 20 msec; this loop needs to be executed 750 times.

Chapter 10

10.7 TRAP occurs since odd address.

10.9(c) Privileged

10.13 $0000 0000

10.16

```
            SWAP        D1
            MOVE        D1,D0
            EXT.L       D0
            SWAP        D1
            EXT.W       D1
            DIVS        D1,D0
FINISH      JMP     FINISH
```

10.18

```
                    MOVE.W D1,D0
                    SWAP       D1
                    ADD     D0,D1
                    SWAP       D1
          FINISH JMP     FINISH
```

10.31 $\overline{AS}$ = 0, FC2FC1FC0 = -1
$\overline{LDS}$ = 1, UDS = 0

10.33 Memory map:
even 2764 $000000,$000002,...,$003FFE
odd 2764 $000001,$000003,...,$003FFF
68230 I/O map:
PGCR = $004001, PADDR = $004005
PBDDR = $004007, PACR = $00400D
PBCR = $00400F, PADR = $004011
PBDR = $004013

Chapter 11

11.6(a) (EAX) = 0000 0080H

11.8

```
MOVSX  CX, BH
IDIV   AX,CX
HLT
```

11.20 (ECX) = 2A157241H

11.22 (AX) = 1234H

11.33 (D1.W) = $4567

11.35
```
CMP.L (0,A0,D5.L*2),D0
```

11.39
```
ADD.L     D3,D0
ADDX.L D2,D1
FINISH   JMP      FINISH
```

11.45 *32-bit device: Byte data will be transferred via 68020 D_{15} - D_8 pins.
*8-bit device: Byte data will be transferred via D_{31} - D_{24} pins.

11.49 GPR0 - GPR31

11.51(b) The PR bit in MSR is 1.

11.52(a The 32-bit contents of r2 and r3 are added; the result is stored in r1. The dot suffix enables the update of the condition register.